What is Claimed Is:

[c1] 1.A data requestor for obtaining requested data from a synchronous data source, the data requestor transmitting for reception by the data source an original clock signal and an original control signal, which is representative of a data request, the data source receiving a delayed version of the original clock signal resulting from a delay in a clock signal path between the data requestor and the data source and a delayed version of the original control signal resulting from a delay in a control signal path between the data requestor and the data source, the data requestor comprising:

a skewed clock signal generator adapted to generate a skewed clock signal that is substantially equivalent to the delayed version of the original clock signal;

a skewed control signal generator adapted to generate a skewed control signal that is substantially equivalent to the delayed version of the original control signal; and

an input sampling module receiving the skewed clock signal and the skewed control signal and being adapted to sample, using the skewed clock signal and the skewed control signal, a data signal to obtain the requested data, wherein the data signal is representative of the requested data and is provided by the data source based at least in part on the delayed versions of the original clock signal and the original control signal.

[c2] 2.The data requestor of Claim 1, wherein the input sampling module is further adapted to perform at least one process operation on the requested data based at least in part on process information associated with the requested data.

[c3] 3.The data requestor of Claim 2, wherein the process information includes one of a group consisting of: a destination of the requested data, a representation of a data type, and reordering information.

[c4] 4.The data requestor of Claim 2, wherein the process information includes a destination of the requested data and the process operation includes providing the requested data to the destination.

[c5] 5.The data requestor of Claim 2, wherein the process information includes a decryption key and the process operation includes decrypting the requested

data using the decryption key.

[c6] 6.The data requestor of Claim 2, further comprising means for providing the process information to the input sampling module synchronously with the skewed clock signal and the skewed control signal.

[c7] 7.The data requestor of Claim 6, wherein the means for providing the process information includes a first dual clock first in-first out (FIFO) buffer in electrical communication with the input sampling module and being adapted to:
store, using the original clock signal, the process information; and
output, using the skewed clock signal, the process information to the input sampling module.

[c8] 8.The data requestor of Claim 6, wherein the means for providing the process information include means for providing the process information to the input sampling module over a process signal path having a delay substantially equivalent to the delay of the clock signal path.

[c9] 9.The data requestor of Claim 1, wherein the skewed clock signal generator includes means for transmitting the original clock signal for reception by the input sampling module over a signal path having a delay that is substantially equivalent to the delay of the clock signal path.

[c10] 10.The data requestor of Claim 1, wherein the skewed control signal generator includes means for providing the original control signal to the input sampling module over a signal path having a delay that is substantially equivalent to the delay of the control signal path.

[c11] 11.The data requestor of Claim 1, further comprising a dual clock FIFO buffer in electrical communication with the input sampling module and being adapted to:
store, using the skewed clock signal, the requested data sampled by the input sampling module; and
provide, using the original clock signal, the requested data to at least one component of the data requestor.

[c12] 12.he data requestor of Claim 1, wherein the data requestor is a memory

controller and the data source is a synchronous memory device.

[c13] 13.An apparatus for synchronizing a data requestor with a data source during a provision of requested data, the data requestor transmitting for reception by the data source an original control signal representative of a data request and an original clock signal and the data source receiving delayed versions of the original clock signal and the original control signal resulting from a delay in a signal path between the data requestor and the data source, the apparatus comprising:
an input sampling module having at least one input and being adapted to:
sample a data signal to obtain the requested data using a skewed clock signal substantially equivalent to the delayed version of the original clock signal and a skewed control signal that is substantially equivalent to the delayed version of the original control signal, wherein the data signal is representative of the requested data and is provided by the data source based at least in part on the delayed versions of the original clock signal and the original control signal; and
perform at least one process operation on the requested data based at least in part on process information associated with the requested data; and
means for providing the process information to the input sampling module synchronously with the skewed clock signal and the skewed control signal.

[c14] 14.The apparatus of Claim 13, wherein the means for providing the process information includes a dual clock FIFO buffer in electrical communication with the input sampling module and being adapted to:
store, using the original clock signal, the process information; and
output, using the skewed clock signal, the process information to the input sampling module.

[c15] 15.The apparatus of Claim 14, further comprising a clock signal skewing circuit adapted to deliver the skewed clock signal for input to the dual clock FIFO buffer and the input sampling module.

[c16] 16.The apparatus of Claim 15, wherein the clock signal skewing circuit communicates the original clock signal to the dual clock FIFO buffer and the input sampling module over a signal path having a delay that is substantially

equivalent to the delay of the signal path between the data requestor and the data source, resulting in the skewed clock signal.

[c17] 17.The apparatus of Claim 13, wherein the process information is communicated to the input sampling module over a signal path having a delay substantially equivalent to the delay between the data requestor and the signal path.

[c18] 18.The apparatus of Claim 13, further comprising a control signal skewing circuit adapted to provide a skewed control signal to the input sampling module.

[c19] 19.The apparatus of Claim 18, wherein the control signal skewing circuit communicates the original control signal to the input sampling module over a signal path having a delay that is substantially equivalent to the delay of the signal path between the data requestor and the data source.

[c20] 20.The apparatus of Claim 13, further comprising a dual clock FIFO buffer in electrical communication with the input sampling module and being adapted to: store, using the skewed clock signal, the requested data sampled by the input sampling module; and provide, using the original clock signal, the output data to at least one component of the data requestor.

[c21] 21.The apparatus of Claim 13, wherein the process information includes one of a group consisting of: a destination of the requested data, a representation of a data type, and reordering information.

[c22] 22.The apparatus of Claim 13, wherein the process information includes a destination of the requested data and the process operation includes providing the requested data to the destination.

[c23] 23.The apparatus of Claim 13, wherein the process information includes a decryption key and the process operation includes decrypting the requested data using the decryption key.

[c24] 24.The apparatus of Claim 13, wherein the data requestor is a memory controller and the data source is at least one synchronous memory device.

[c25] 25.A memory controller for obtaining stored data from a synchronous memory device, the memory controller transmitting for reception by the memory device a first clock signal and a first control signal representative of a data request, the memory device receiving a delayed version of the first clock signal resulting from a delay in a clock signal path between the memory controller and the memory device and a delayed version of the first control signal resulting from a delay in a control signal path between the memory controller and the memory device, the memory controller comprising:

a clock signal skewing circuit for communicating the first clock signal over a clock signal skew path having a delay substantially equivalent to the delay of the clock signal path, whereby the clock signal skewing circuit delivers a second clock signal representative of the delayed version of the first clock signal;

a control signal skewing circuit for communicating the first control signal over a control signal skew path having a delay substantially equivalent to the delay of the control signal path, whereby the control signal skewing circuit delivers a second control signal representative of the delayed version of the first control signal;

a first dual clock FIFO buffer in electrical communication with the clock signal skewing circuit and being adapted to: store, using the first clock signal, process information associated with the stored data; and output, using the second clock signal, the process information; and

an input sampling module in electrical communication with the clock signal skewing circuit and the first dual clock FIFO buffer, the input sampling module being adapted to:

sample a data signal based at least in part on the second clock signal and the second control signal, wherein the data signal is representative of the stored data and is provided by the memory device based at least in part on the second clock signal and second control signal;

obtain the process information from the first dual clock FIFO buffer based at least in part on the second clock signal and the second control signal; and

perform at least one process operation on the stored data based at least in part on the process information.

[c26] 26.The memory controller of Claim 25, further comprising a second dual clock FIFO buffer in electrical communication with the input sampling module and being adapted to:
store, using the skewed clock signal, the stored data sampled by the input sampling module; and
provide, using the original clock signal, the stored data to at least one component of the memory controller.

[c27] 27.The memory controller of Claim 25, wherein the process information includes one of a group consisting of: a destination of the stored data, a representation of a data type, and reordering information.

[c28] 28.The memory controller of Claim 25, wherein the process information includes a destination of the stored data and the process operation includes providing the stored data to the destination.

[c29] 29.The memory controller of Claim 25, wherein the synchronous memory device includes one of a group consisting of: SDRAM, SSRAM, a synchronous FIFO, and programmable logic.

[c30] 30.A method for synchronizing a data requestor with a data source during a transfer of requested data, the method comprising the steps of:
generating a skewed clock signal approximating a delayed version of an original clock signal communicated to the data source, the delayed version resulting at least in part from delay associated with a clock signal path over which the original clock signal is transmitted between the data requestor and the data source;
generating a skewed control signal approximating a delayed version of an original control signal communicated to the data source, the delayed version resulting at least in part from delay associated with a control signal path over which the original control signal is transmitted between the data requestor and the data source; and
sampling, using the skewed clock signal and skewed control signal, a data signal received by the data requestor from the data source to obtain the requested data.

[c31] 31.The method of Claim 30, further comprising the steps of:
obtaining, using the skewed clock signal, process information associated with the requested data; and
performing, at the data requestor, at least one process operation on the requested data based at least in part on the process information.

[c32] 32.The method of Claim 31, wherein the process information includes one of a group consisting of:
a destination of the stored data, a representation of a data type, and reordering information.

[c33] 33.The method of Claim 31, wherein the process information includes a destination of the stored data and the step of performing the at least one process operation includes providing the stored data to the destination.

[c34] 34.The method of Claim 31, further comprising the step of storing, using the original clock signal, the process information in a dual clock FIFO buffer.

[c35] 35.The method of Claim 34, wherein the step of obtaining the process information includes obtaining the process information from the dual clock FIFO buffer using the skewed clock signal and the skewed control signal.

[c36] 36.The method of Claim 31, wherein the step of obtaining the process information includes transmitting the process information over a signal path having a delay substantially equivalent to a delay between the original clock signal and the delayed version of the original clock signal.

[c37] 37.The method of Claim 30, wherein the step of generating the skewed clock signal includes transmitting the original clock signal over a signal path having a delay that is substantially equivalent to a delay over a clock signal path used to transmit the original clock signal from the data requestor to the data source.

[c38]

38.The method of Claim 30, wherein the step of generating the skewed control signal includes transmitting the original control signal over a signal path having a delay that is substantially equivalent to a delay over a control signal path used to transmit the original control signal from the data requestor to the data

source.

[c39] 39.The method of Claim 30, further comprising the step of storing, using the skewed clock signal, the requested data in a dual clock FIFO buffer.

[c40] 40. The method of Claim 39, further comprising the step of retrieving, using the original clock signal, the stored data from the dual clock FIFO buffer.

[c41] 41.A method for synchronizing a memory controller with a synchronous memory device during a read access of stored data, the method comprising the steps of:
sampling, using a second clock signal and a second control signal, a data signal provided by the memory device to obtain the stored data, the second clock signal being representative of a delayed version of a first clock signal received by the memory device from the memory controller and the second control signal being representative of a delayed version of a first control signal received by the memory device from the memory controller;
obtaining, using the second clock signal, process information associated with the stored data from a first dual clock FIFO buffer; and
performing at least one process operation on the stored data based at least in part on the process information.

[c42] 42.The method of Claim 41, further comprising the step of storing, using the first clock signal, the process information in the first dual clock FIFO buffer.

[c43] 43.The method of Claim 42, further comprising the step of generating the process information.

[c44] 44.The method of Claim 41, further comprising the steps of:
generating the second clock signal from the first clock signal; and
generating the second control signal from the first control signal.

[c45] 45.The method of Claim 44, wherein the step of generating the second clock signal includes transmitting the first clock signal over a signal path having a delay that is substantially equivalent to a delay over a clock signal path used to transmit the first clock signal from memory controller to the synchronous

memory device.

[c46] 46.The method of Claim 45, wherein the step of generating the second control signal includes transmitting the first control signal over a signal path having a delay that is substantially equivalent to a delay over a control signal path used to transmit the first control signal from the memory controller to the synchronous memory device.

[c47] 47.The method of Claim 41, further comprising the step of storing, using the second clock signal, the stored data in a second FIFO buffer.

[c48] 48.The method of Claim 47, further comprising the step of retrieving, using the first clock signal, the stored data from the second FIFO buffer.

[c49] 49.The method of Claim 41, wherein the process information includes one of a group consisting of:
a destination of the stored data, a representation of a data type, and reordering information.

[c50] 50.The method of Claim 41, wherein the process information includes a destination of the stored data and the step of performing the at least one process operation includes providing the stored data to the destination.

[c51] 51.The method of Claim 41, wherein the process information includes a decryption key and the step of performing the at least one process operation includes decrypting the stored data using the decryption key.

[c52] 52.In a digital subscriber line modem comprising a communications processor coupled to a synchronous memory device, the communications processor transmitting for reception by the memory device an original control signal representative of a data request and an original clock signal and the memory device receiving a delayed version of the original clock signal resulting from a delay in a clock signal path between the communications processor and the memory device and a delayed version of the original control signal resulting from a delay in a control signal path between the communications processor and the memory device, an apparatus for synchronizing an access of the

requested data stored in the memory device comprising:
means for generating a skewed clock signal substantially equivalent to the delayed version of the original clock signal;
means for generating a skewed control signal substantially equivalent to the delayed version of the original control signal; and
an input sampling module in electrical communication with the means for generating the skewed clock signal and the means for generating the skewed control signal and being adapted to sample, using the skewed clock signal and the skewed control signal, a data signal to obtain the requested data, wherein the data signal is representative of the requested data and is provided by the data source based at least in part on the delayed versions of the original clock signal and the original control signal.